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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,178	03/19/2004	Shiro Yamagishi	61282-067	6750

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EXAMINER	
CHEN, ALAN S	
ART UNIT	**PAPER NUMBER**
2182	

MAIL DATE	DELIVERY MODE
12/10/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/804,178	YAMAGISHI, SHIRO	
	Examiner	Art Unit	
	Alan S. Chen	2182	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/23/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09/27/07 has been entered.

Response to Arguments

2. Applicant's arguments with respect to claim have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

3. Claim 5 is objected to because of the following informalities: the term –DMA– is still misspelled "DMS". Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 and 2 are rejected under 35 USC 103(a) as being unpatentable over US Pat. Pub. No. 2002/0026543 to Tojima et al. *(Tojima, cited previously)* in view of US Pat. No. 5,430,844 to Shitara et al. *(Shitara)*.

6. Per claim 1, Tojima discloses a DMA controller *(Fig. 1, element 101)* which generates ring buffer addresses *(Fig. 17, parameter memory has various addresses related to ring buffer)*, comprising: a first memory, which sets the start address of a ring buffer *(Fig. 17, memory element for ring buffer 2 area has start address for both read and writes)*, a second memory, which sets the number of DMA transfers from the start address to the end address of the ring buffer *(Fig. 17, memory element for ring buffer 2 area has number of transfers for both read and write)*.

Tojima does not disclose expressly the parameter memory is in register form or having a and a third register, which sets the difference between the end address and the start address of the ring buffer.

Shitara discloses it is well-known to one of ordinary skill in the art that DMA transfers require the size of the total DMA transfer (Column 1, lines 58-62, DMA transfer generally require two registers, one for address and another for size). This is equivalent to the difference of the start address and end address. In Shitara, the start address is stored and the size of the transfer is also stored, therefore there is no need for the end address. This is simply a matter of design choice. The end address would be redundant.

Tojima and Shitara are analogous art because they are from the same field of endeavor in transfer data via DMA.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use registers and have a register that represents the difference of the start and end addresses.

The suggestion/motivation for doing so would have been register use to store significant and widely used values well-known. Values such as the start address will change and will be accessed for various DMA transfers. The transfer size is one of the fundamental values for DMA transfers as suggested by Shitara and is therefore useful to include in a register. Note, Tojima discloses does not preclude parameter memory as being several registers or a register file.

7. Per claim 2, Tojima combined with Shitara discloses claim 1, Tojima further disclosing a second rectangular mode *(paragraph 252)* wherein the second register is used as a register for setting the number of DMA transfers in a contiguous area *(paragraph 253)* including rectangular areas in the DMA transfer of a rectangular area included in an area *(paragraph 252-254)*.

8. Claims 3-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tojima in view of Shitara in further view of U.S. Patent 5,708,849 to Coke et al. *(Coke, previously cited)*.

9. Per claim 3, Tojima combined with Shitara fails to teach the address increment of a non-contiguous area. Coke teaches the third register is used as a register for setting the address increment of a non-contiguous area in the DMA transfer of a rectangular area included in an area *(incrementer, Fig. 3, element 39, column 5, liens 65-69)*. It would have been obvious to one of ordinary skill in the art to combine the amount of information to be transferred of Coke with the DMA controller of Tojima combined with Shitara in order to reduce the processor load on the system.

10. Per claim 4, Tojima combined with Shitara fails to teach, but Coke teaches a fourth register, which retains a current transfer address *(Fig. 3, element 35)*, a counter which counts the number of DMA transfers set to the second register *(Fig. 3, element 36)*, and an adder, which sums the value of the third register and the value of the fourth register when the counter has completed counting the number of DMA transfers set to the second register *(Fig. 3, element 39)*. It would have been obvious to one of ordinary skill in the art to combine the length information of Baxter and increment information of Coke with the DMA controller of Tojima combined with Shitara in order to reduce the processor load on the system.

11. Per claim 5, Tojima combined with Shitara teaches the limitations of previous rejected claims 1 and 2. The computer readable media is represented by the pertinent memory elements of Fig. 1 in Tojima, which have instructions in a program to actuate the DMA controller. Tojima combined with Shitara does not clearly teach means for setting the address increment of a non-contiguous area to the third register. Coke teaches that setting the address increment of a non-contiguous area to the third register *(Figs. 3 and 6, column 5, line 48, though column 8, line 47)*. It would have been obvious to one of ordinary skill in the art to combine the size/length information of Shitara and increment information of Coke with the DMA controller of Tojima in order to reduce the processor load on the system.

12. Per claim 6, Tojima combined with Shitara and Coke disclose claim 3, Tojima further teaches a first mode of operation corresponds to a ring buffer transfer, and said second mode of operation corresponds to a rectangular block transfer *(paragraph 42)*.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan S. Chen whose telephone number is 571-272-4143. The examiner can normally be reached on M-F 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Henry Tsai can be reached on 571-272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ASC
12/01/07